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(81) Designated States (*national*): CN, JP, KR, US.

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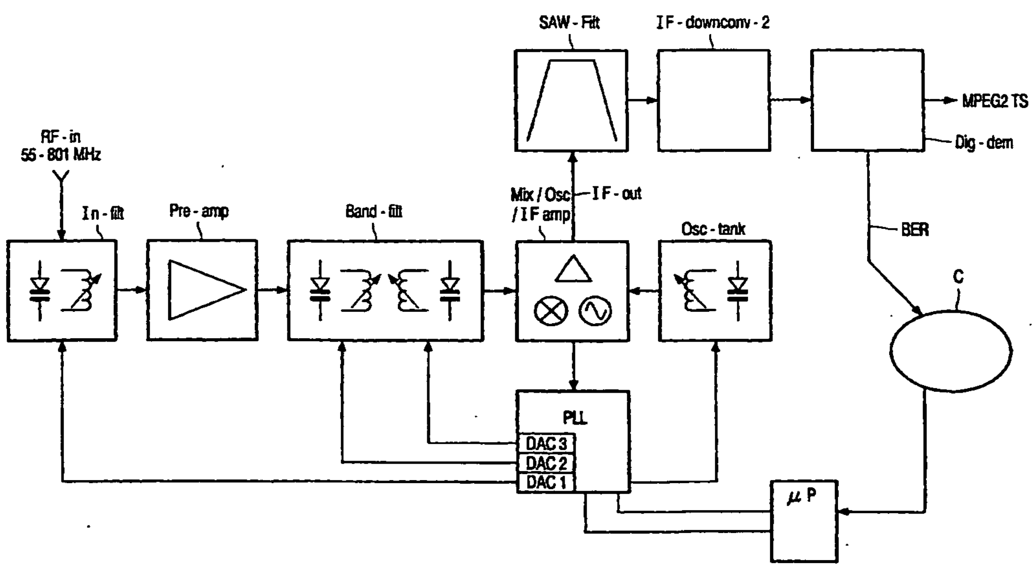
(54) Title: TUNER ALIGNMENT



(57) Abstract: In a method of tuning a receiver for a digital signal (MPEG2-TS), an input signal (RF-in) is filtered (In-filt, Band-filt) to obtain a processed signal, a digital figure of merit (BER) is determined (Mix/Osc/IF amp IF-downconv-2, C) from the processed signal, and the filtering step (In-filt, Band-filt) is fine-adjusted (µP, PLL, DAC1-DAC3) in dependence on the digital figure of merit (BER).

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Tuner alignment.

The invention relates to a tuning method and a receiver for a digital signal, such as an MPEG2 transport stream.

The article "Fully automatic self alignment of TV-tuners", by Gerd M. Maier, in IEEE Transactions on Consumer Electronics, Vol. CE-32, No. 3, August 1986, pp. 302-305, discloses a dynamic alignment system that consists of an oscillator, a PLL system, 3x6 bit D/A converters, a mixer, and a sample and hold circuit. The alignment process is started by selecting the desired TV channel. The PLL data, which sets the tuner oscillator to the correct frequency, will be calculated and PLL data stored. The RF filter alignment is carried out as follows. An input transistor stage receives an AGC voltage of around 1 V in order to block all antenna signals from the RF 2-pole filter. The secondary filter will be set to either 1 or 30 V, the primary filter initialized, and the alignment subroutine activated. Following the alignment of the primary filter to maximum, it will be set to either 1 or 30 V. Then the secondary filter is initialized and again the alignment subroutine is activated. After this procedure is finished, the primary filter will be set to its proper tuning voltage value. The PLL is set to PLL +2.75 MHz in case of the German TV standard, where a 5.5 MHz difference exists between the picture and sound carrier frequencies. The AGC goes to 7V to allow maximum gain (uncontrolled) in the input stage. The antenna filter is initialized and again the alignment routine started; after this run is completed the PLL goes to PLL –2.75 MHz which is the correct oscillator frequency for the desired TV channel. The alignment is finished and the TV set brought back in the received mode.

Every channel change incurs a total re-alignment of the tuner in such a manner, that when one filter is being aligned, the others are put in a reference state. An analysis of a prototype showed that the whole alignment procedure is finished within 300 ms, which is relatively long. Considering that in a digital receiver there are more loops to be locked than just the RF receiver block and that this block is the main contributor to the channel switching time, even the current 150 ms specified for tuners may be too slow. In addition, the tuner alignment sequence seems not to take into account the response of the signal arriving at the antenna input, which may not be nominally flat. This prior art solution also calls for an

additional mixer block to generate the signal needed for alignment of the primary and secondary tuner circuits.

Single conversion tuners make use of sets of tracking filters to suppress unwanted signals before converting the incoming signal to the intermediate frequency. Due to the range of coverage of the filters, wide ranging impedance and varying Q values with frequency, it is difficult to maintain consistent frequency response without incurring tremendous cost increase in terms of material and process.

EP-A-0,176,144 discloses a television receiver comprising an automatic radio-frequency resonant circuit adjustment circuit. Use is made of two carriers fed to a read frequency input of the receiver, and the product of the amplitudes of the two carriers is formed by means of a detection circuit coupled to an output of the radio-frequency resonant circuit. The adjustment setting of the resonant circuit is effected to a maximum value of this product, thus providing a correct adjustment in a simple way for analog signals.

It is, inter alia, an object of the invention to provide an improved tuner filter alignment for use with digital signals. To this end, the invention provides a tuning method and a receiver for a digital signal as defined in the independent claims. Advantageous embodiments are defined in the dependent claims.

In a method of tuning a receiver for a digital signal in accordance with a primary aspect of the present invention, an input signal is filtered to obtain a processed signal, a digital figure of merit is determined from the processed signal, and the filtering step is fine-adjusted in dependence on the digital figure of merit. The digital figure of merit may be a bit-error rate. Preferably, the digital figure of merit is a signal quality indicator signal generated in conformity with our non-prepublished US patent application no. 09/282,322, filed on March 31, 1999 (Attorneys' docket PHA 23.641).

It is noted that the use of a bit-error rate is known as such from completely different types of circuits. US-A-4,639,682 discloses a carrier reproducing circuit for phase shift keying signals. A frequency converter converts the frequency of a PSK signal into a frequency of a carrier to be reproduced. A carrier reproducing circuit includes a PLL circuit that reproduces the carrier. The intended data in the reproduced carrier is demodulated. A frequency correction data generator forms correction data according to a bit-error rate of the demodulated data, and superposes the correction data on a control voltage to a voltage controlled oscillator of the PLL circuit.

US-A-5,065,107 discloses a phase-locked loop bandwidth switching demodulator for suppressed carrier signals. A variable frequency oscillator is responsive to a control signal for oscillating at a frequency corresponding to an intermediate frequency. A frequency difference detector produces an output signal indicative of the frequency difference between the frequency of the input signal and the intermediate frequency. A feedback loop network has a narrow-band path and a wide-band path and is responsive to a detector output signal for producing a control signal and applying the control signal to an oscillator through one of the paths whereby to change the intermediate frequency of the oscillator in response to the control signal. A quality detector is responsive to the detector output signal for producing a signal corresponding to a bit-error rate of the input signal. A selection means is responsive to the bit-error rate signal for causing the control signal to pass through the narrow-band path when the bit-error rate signal is below a predetermined threshold, and through the wide-band path when the bit-error rate signal exceeds the predetermined threshold.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

The drawing shows an embodiment of a tuner in accordance with the present invention.

The invention is based on the recognition that a dynamic fine-tuning of the RF response of a tuner can overcome the above-mentioned limitation of a single conversion tuner and in effect even compensate for distortions in the transmission network. The idea calls for a tuner that is aligned much in the normal way, by manually adjusting wire-wound air-coils. Assuming that this already brings the performance to about 80% right, then fine-tuning can deliver the remaining 20%. The 80% performance level of the RF response is likely sufficient for a digital receiver to acquire lock and for synchronization to take place. Tuner alignment improvement is then a matter of individually tuning the RF circuits until a digital figure of merit (for example, the bit-error rate) reaches its best value.

The drawing shows an embodiment of a tuner in accordance with the present invention. An RF input signal RF-in (55..801 MHz) is applied to an input filter In-filt. Its output signal is applied to a double tuned band-filter Band-filt thru a pre-amplifier Pre-amp. An output signal of the double tuned band-filter Band-filt is applied to a mixer / oscillator / IF amplifier circuit Mix/Osc/IF amp forming a tuner mixer stage that furnishes the IF output

signal IF-out at e.g. 45.75 MHz. Another output of the mixer / oscillator / IF amplifier circuit Mix/Osc/IF amp is coupled to an input of a PLL IC with multiple tuning voltage outputs. The PLL circuit controls the input filter In-filt, the double tuned band-filter Band-filt, and an oscillator tank circuit Osc-tank forming the tuner local oscillator and having an output coupled to the mixer / oscillator / IF amplifier circuit Mix/Osc/IF amp. The coils are used for factory alignment. They are opened or closed (pushed with a stick) until a desired response is achieved.

The IF output signal IF-out is applied to a second IF down-converter IF-downconv-2 thru a SAW filter SAW-filt. An output of the second IF down-converter IF-downconv-2 is coupled to a digital demodulator Dig-dem that furnishes, for example, an MPEG-2 transport stream MPEG2 TS. The digital demodulator Dig-dem contains an equalizer.

Error information such as a bit-error rate BER or, preferably, a signal quality indicator signal generated in conformity with our non-prepublished US patent application no. 09/282,322, filed on March 31, 1999, Attorneys' docket PHA 23.641, (made) available in the digital demodulator Dig-dem is applied to a micro-processor μP after an optional conditioning in a conditioning block C. The micro-processor μP controls three D/A converters DAC1, DAC2 and DAC3 contained in the PLL IC in accordance with the algorithm set out below.

A preferred fine-tuning algorithm comprises the following steps:

1. Change to a new channel. If there is no lock, signal an error. If there is a lock, go on with the following steps.
2. Fine-tune DAC1 that controls the input filter.
3. Fine-tune DAC2 that controls the primary filter of the double-tuned band-filter.
4. Fine-tune DAC3 that controls the secondary filter of the double-tuned band-filter.

Each of the fine-tuning actions 2-4 comprises the following steps:

a. Increase the DAC offset. If this reduces the bit-error rate, repeat this step a.
b. Decrease the DAC offset. If this reduces the bit-error rate, repeat this step b.
c. Increase the DAC offset.

So, when a channel change is triggered, the tuner receives the standard command via an inter-IC bus (I^2C) to change band (if necessary) and tune the oscillator to the

correct oscillator frequency. At this point, picture is available, even though the specified RF response flatness and/or bit-error rate threshold for quasi-error-free (QEF) is not yet reached.

Keeping the primary and secondary circuits of a tuner as they are, the center frequency of the input filter In-filt is varied by means of an offset on DAC1. This moves first in a positive direction. Assuming that the positive offset resulted in an improvement (decrease) of the bit-error rate, then this should continue until the bit-error rate reaches its point of inflection (minimum). If increasing the offset results in a worsening bit-error rate, then the control starts decreasing the offset until the point of inflection is found. Because finding an inflection point requires departing from the optimal setting, the last step is to make a positive offset before branching back to the main routine.

The same is repeated for DAC2 and DAC3 connected to the primary and secondary bandpass circuits of the double-tuned band-filter Band-filt of the tuner, respectively.

At the end of the exercise, the tuner alignment is at best. Given the characteristics of the transmission system, it is hypothesized that the frequency response will be virtually at its most flat in case there are no interferences or signal impairments, or a maximum rejection of an undesired interfering signal, usually one or more channels away, is obtained at an RF response curve that will be far from flat.

One of the considerations is that the offset change steps taken by the DACs cannot be too large as to cause too severe a change in the response. In the worst case, synchronization could be lost. An optimal fine-tuning can be obtained with variable offset sizes at different frequency points.

In this preferred embodiment, the filters are aligned successively. When the first filter is aligned, the second and third filters are in the factory pre-aligned state. When the second filter is aligned, the first filter is in the fine-aligned state while the third filter is in the factory pre-aligned state. When the third filter is aligned, both the first and second filters are in the fine-aligned state.

Preferably, a pre-alignment is carried out "in-factory" by applying a swept signal at the input of the device and detecting the output. This output (which is the superposition of the 3 sets of filter response and in some cases an additional IF filter) is tuned manually by pushing/stretching wire wound air coils with DAC offset voltages set to 0. This procedure is in fact the same as that carried out for standard tuners produced today. The pre-aligned tuner supports the fast acquisition of signals, which is an important point of consideration in TV applications.

A preferred embodiment of the invention is formed by a receiver block with a tuner utilizing a PLL IC with multiple DACs. This allows each tuned circuit in the tuner to be independently tuned. By monitoring an error signal downstream of the receiver chain, the individual tuning voltages can be manipulated so as to arrive at the optimum alignment for best signal quality.

For an analog TV system a direct link exists between channel (tuner) tilt and video response. For any of the digital modulation schemes this is, however, no longer the case. Tilt will translate in a loss of receiver margin, one of which for example the sensitivity. If one looks at the spectral shape of multi-path RF signals arriving at the input of a digital terrestrial receiver you will find severe distortions, way beyond what can be corrected for by the digital demodulator (equalizer). So, rather than fine tuning the RF response to maximum flatness, the invention offers the ability to improve receiving conditions by deliberately distorting the tuner RF response. This (linear) distortion serves the purpose of creating more favorable signal conditions at the tuner mixer stage and the IF SAW driver. This can, however, only work in conjunction with an equalizer further on in the chain, which equalizer again eliminates the distortions of the desired signal. Take for example an N-2 interference condition. By moving the RF response curve in its totality nearer to the Local Oscillator (shift all RF circuits in tandem) a (probably considerable) amount of additional selectivity can be achieved. Same so for any other taboo channel the rejection of which relies on RF selectivity. The essential difference with a standard tuner is that for the latter there is a limit to the attainable selectivity induced by need for flat RF response, component tolerance (varicaps) and alignment inaccuracy. A dynamically optimized RF response may allow better overall results without making tuner a lot more expensive. So, depending on the signal conditions, the best optimized response may not look like what we are familiar with (i.e. a flat symmetrical response) but could instead be a skewed curve to favor the desired signal and block out (attenuate) any strong interferences.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a

plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A method of tuning a receiver for a digital signal (MPEG2-TS), the method comprising the steps of:

filtering (In-filt, Band-filt) an input signal (RF-in) to obtain a processed signal;

determining (Mix/Osc/IF amp, IF-downconv-2, Dig-dem, C) a digital figure of merit (BER) from the processed signal; and

fine-adjusting (μP, PLL, DAC1-DAC3) the filtering step (In-filt, Band-filt,) in dependence on the digital figure of merit (BER).

2. A method as claimed in claim 1, wherein the digital figure of merit (BER) is a bit-error rate.

3. A method as claimed in claim 1, wherein

the filtering step (In-filt, Band-filt) comprises at least one partial filtering step that is controlled by a control signal; and

the fine-adjusting step (μP, PLL, DAC1-DAC3) comprises the step of adjusting the control signal in order to optimize the figure of merit.

4. A method as claimed in claim 1, wherein

the filtering step (In-filt, Band-filt) comprises at least two partial filtering steps that are controlled by at least first and second respective control signals; and

the fine-adjusting step (μP, PLL, DAC1-DAC3) comprises the steps of adjusting the first control signal in order to optimize the digital figure of merit, to obtain an adjusted first control signal value, and, while the first control signal is kept at the adjusted first control signal value, adjusting the second control signal in order to optimize the digital figure of merit.

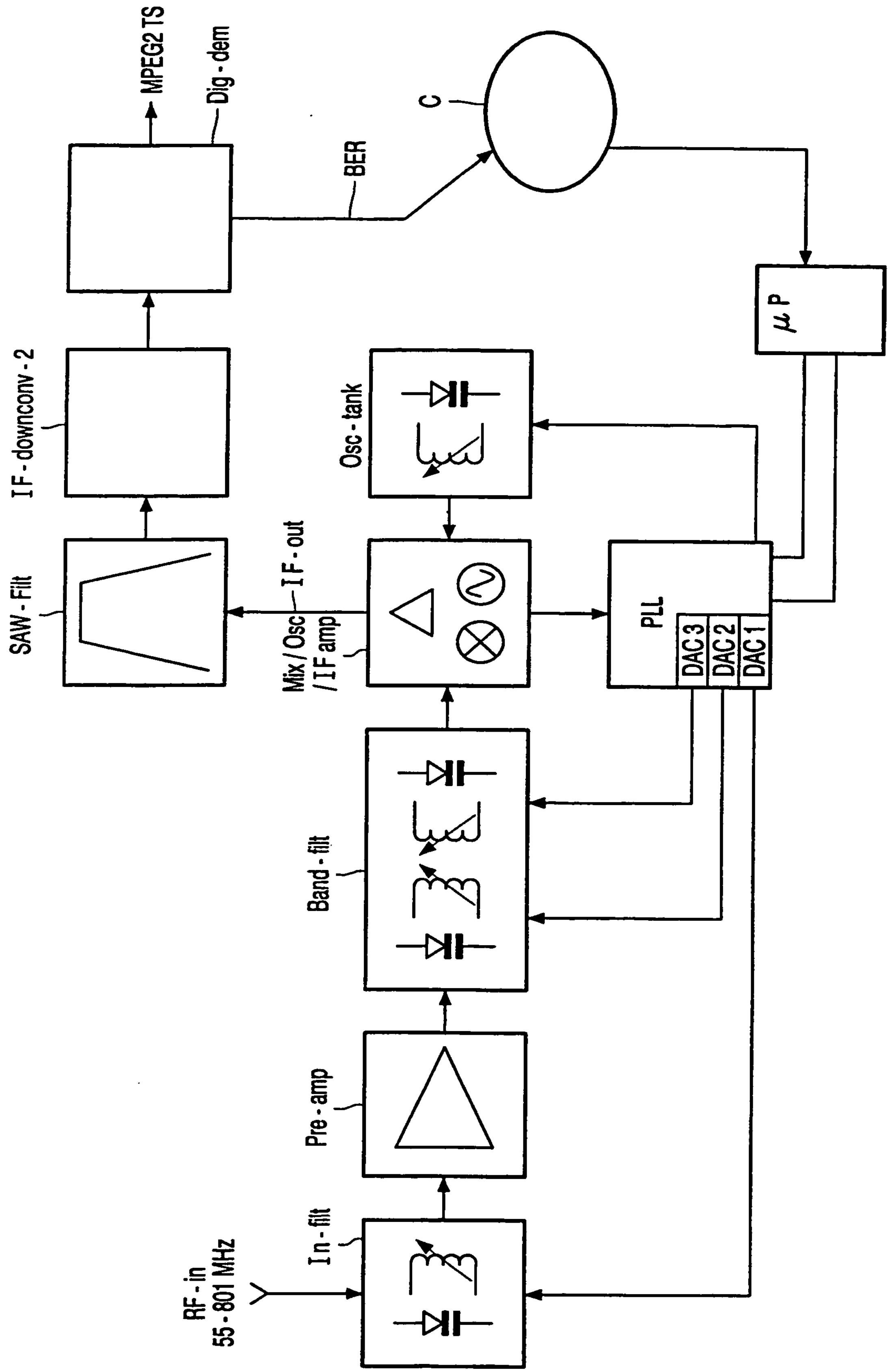
5. A method as claimed in claim 1, wherein the filtering step (In-filt, Band-filt) uses circuitry that is factory pre-aligned.

6. A receiver for a digital signal (MPEG2-TS), the receiver comprising:

means for filtering (In-filt, Band-filt) an input signal (RF-in) to obtain a processed signal;

means for determining (Mix/Osc/IF amp, IF-downconv-2, Dig-dem, C) a digital figure of merit (BER) from the processed signal; and

means for fine-adjusting (μP, PLL, DAC1-DAC3) the filtering means (In-filt, Band-filt) in dependence on the digital figure of merit.


MPEG2 TS
Dig - dem
BER
C
μ P
I F - downconv - 2
Osc - tank
SAW - Filt
I F - out
Mix / Osc / I F amp
PLL
DAC 3
DAC 2
DAC 1
Band - filt
Pre - amp
In - filt
RF - in
55 - 801 MHz

09/890,490

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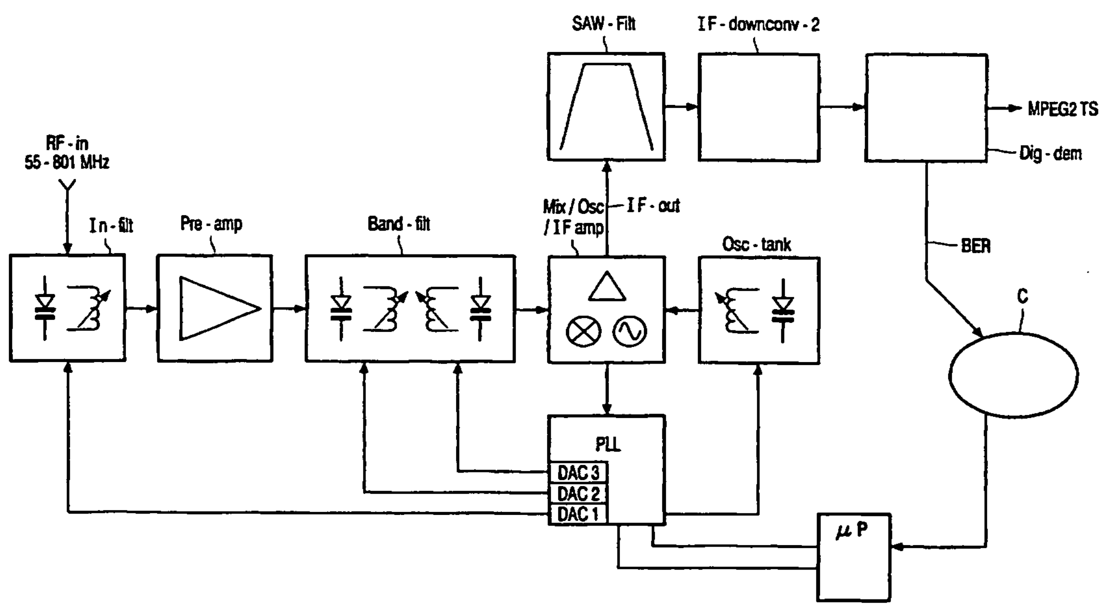

(57) Abstract: In a method of tuning a receiver for a digital signal (MPEG2-TS), an input signal (RF-in) is filtered (In-filt, Band-filt) to obtain a processed signal, a digital figure of merit (BER) is determined (Mix/Osc/IF amp IF-downconv-2, C) from the processed signal, and the filtering step (In-filt, Band-filt) is fine-adjusted (μP, PLL, DAC1-DAC3) in dependence on the digital figure of merit (BER).

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 00/11826

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 404 161 A (DOUGLASS RALPH G ET AL) 4 April 1995 (1995-04-04)	1,3,4,6
Y	column 4, line 50 -column 20, line 26	2

Y	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 04, 31 March 1998 (1998-03-31) & JP 09 326837 A (KOKUSAI ELECTRIC CO LTD), 16 December 1997 (1997-12-16) abstract	2

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 June 2001	03/07/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Materne, A

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 00/11826

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5404161 A	04-04-1995	AU 7330294 A	28-02-1995
		WO 9504429 A	09-02-1995
		US 5510859 A	23-04-1996
JP 09326837 A	16-12-1997	NONE	

PATENT COOPERATION TREATY

PCT

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PHN 17.751WO	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/EP 00/ 11826	International filing date *(day/month/year)* 27/11/2000	(Earliest) Priority Date *(day/month/year)* 01/12/1999
Applicant KONINKLIJKE PHILIPS ELECTRONICS N.V.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

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[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

[X] the text is approved as submitted by the applicant.

[ ] the text has been established by this Authority to read as follows:

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[ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

[X] as suggested by the applicant.

[ ] because the applicant failed to suggest a figure.

[ ] because this figure better characterizes the invention.

[ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 June 2001	03/07/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Materne, A

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JP 09326837 A	16-12-1997	NONE	

Patent Abstracts of Japan

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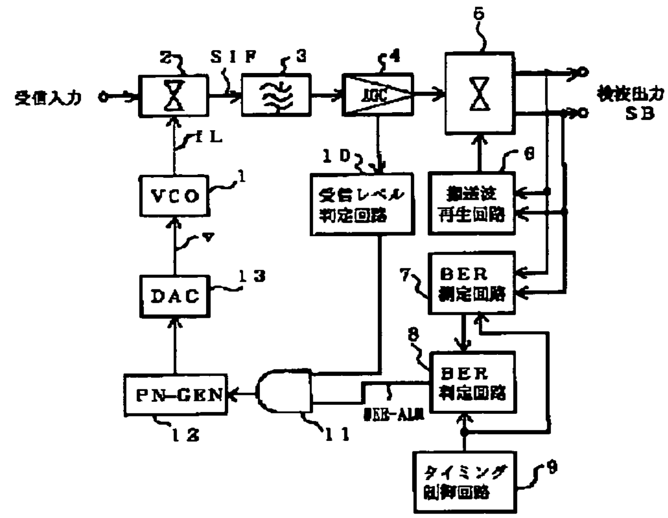
TITLE : AUTOMATIC FREQUENCY CONTROL METHOD, CIRCUIT THEREFOR AND RECEIVER



ABSTRACT : PROBLEM TO BE SOLVED: To realize the stable small sized automatic frequency control circuit at a low cost.

SOLUTION: Transmission data including error rate measurement data are transmitted and an error rate measurement circuit 7 measures an error rate of the measurement data. An error rate discrimination circuit 8 provides an output of a signal BER-ALM when the measured error rate is a prescribed value or over. This signal passes through a gate 11 to start a pseudo random signal generator 12 when a reception level discrimination circuit 10 discriminates that the reception level is a prescribed level or over. A pulse train outputted from the started generator 12 is given to a D/A converter 13, in which the pulse train is converted into a DC voltage (v) and the frequency of a local oscillation circuit 1 receives random fluctuation. As a result, when the error rate measured by the error rate measurement circuit 7 reaches a prescribed rate or below, the control above is finished and a carrier with a desired frequency is outputted from a local oscillation circuit.